FIG. 1

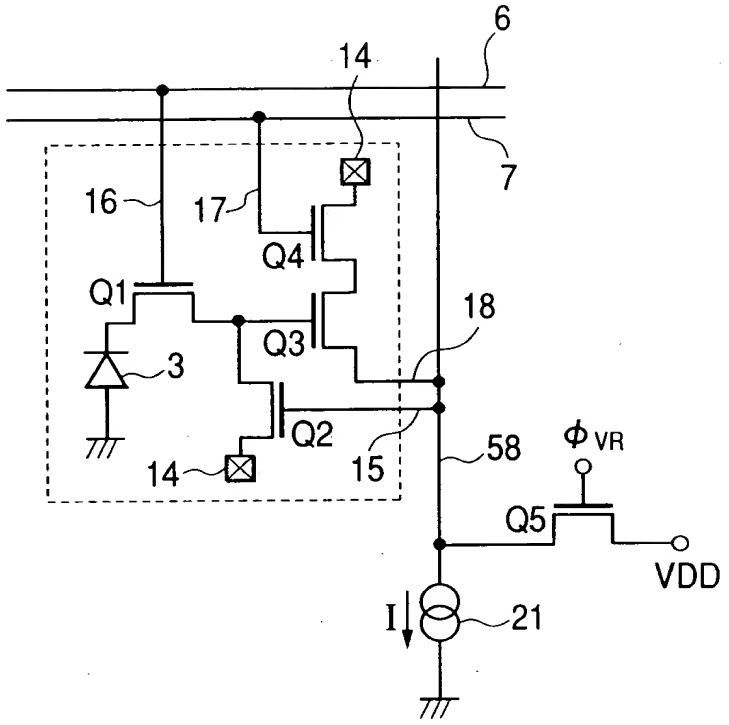
6
14
7
16
17
Q4
Q1
18
Q3
3
Q2
14
15
58
ϕ VR
Q5
VDD
I
21

FIG. 2

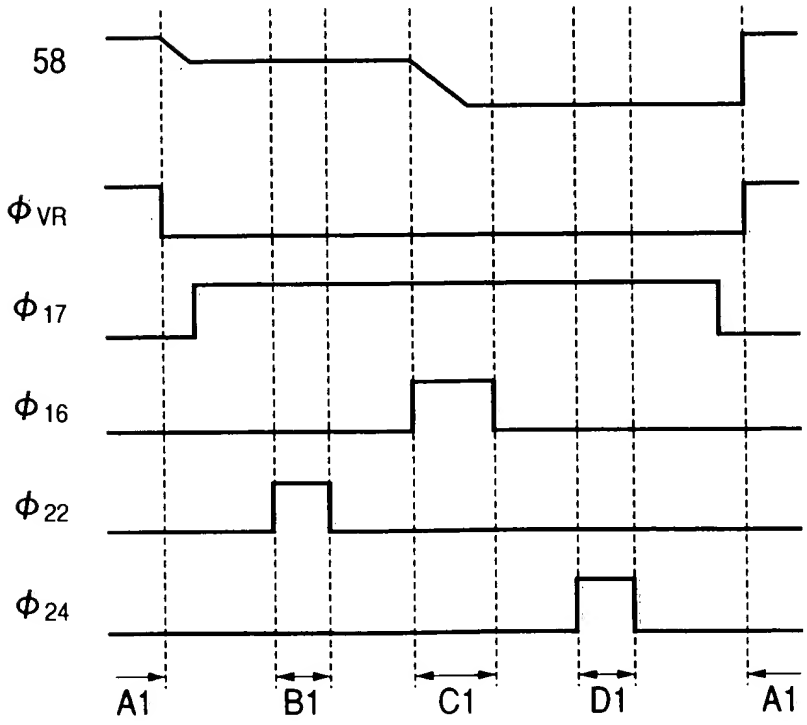
58
ϕ VR
ϕ 17
ϕ 16
ϕ 22
ϕ 24
A1
B1
C1
D1
A1

FIG. 3

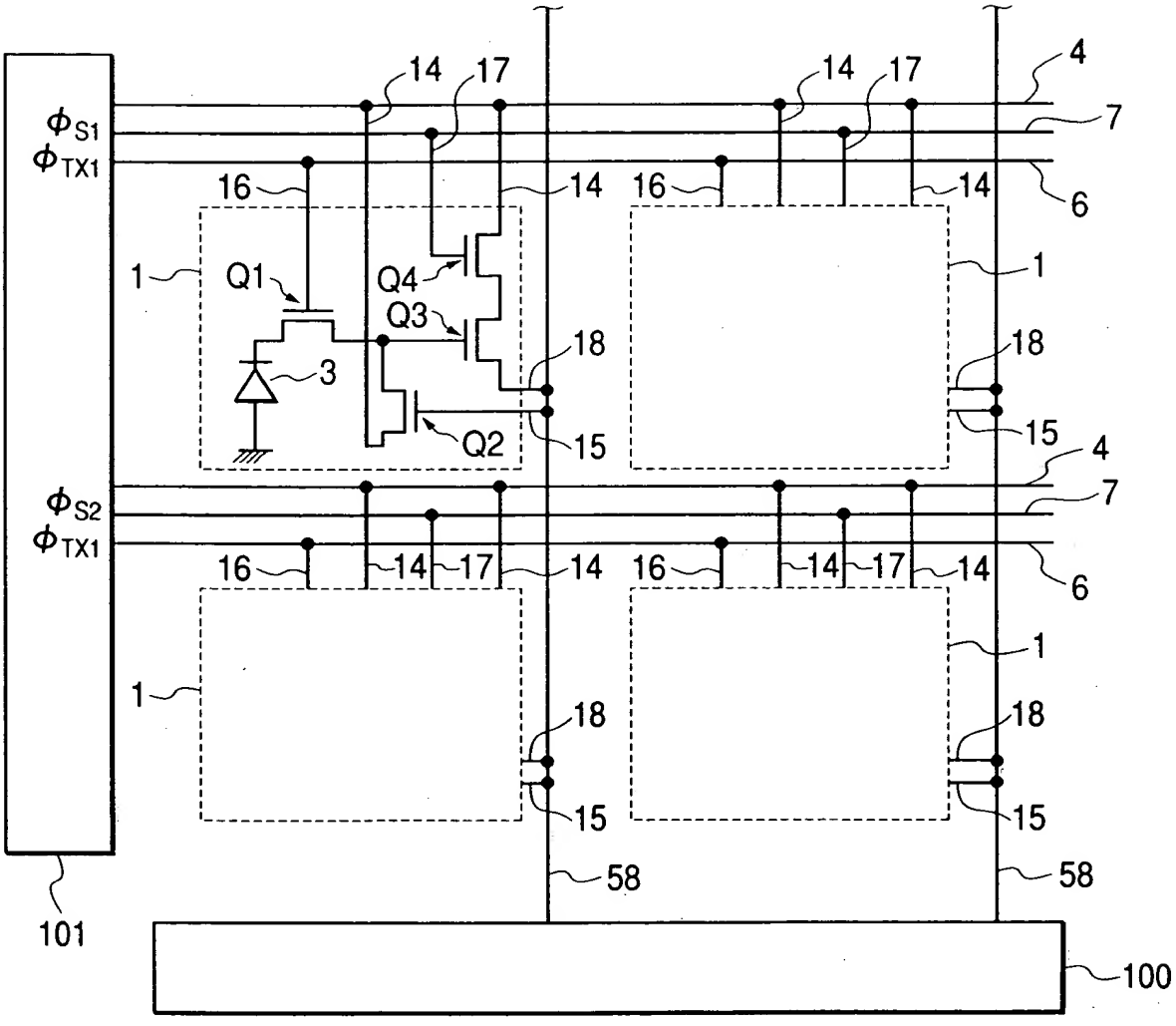
ϕ_{S1}
ϕ_{TX1}
ϕ_{S2}
ϕ_{TX1}
Q1
Q2
Q3
Q4
1
3
4
6
7
14
15
16
17
18
58
100
101

FIG. 4

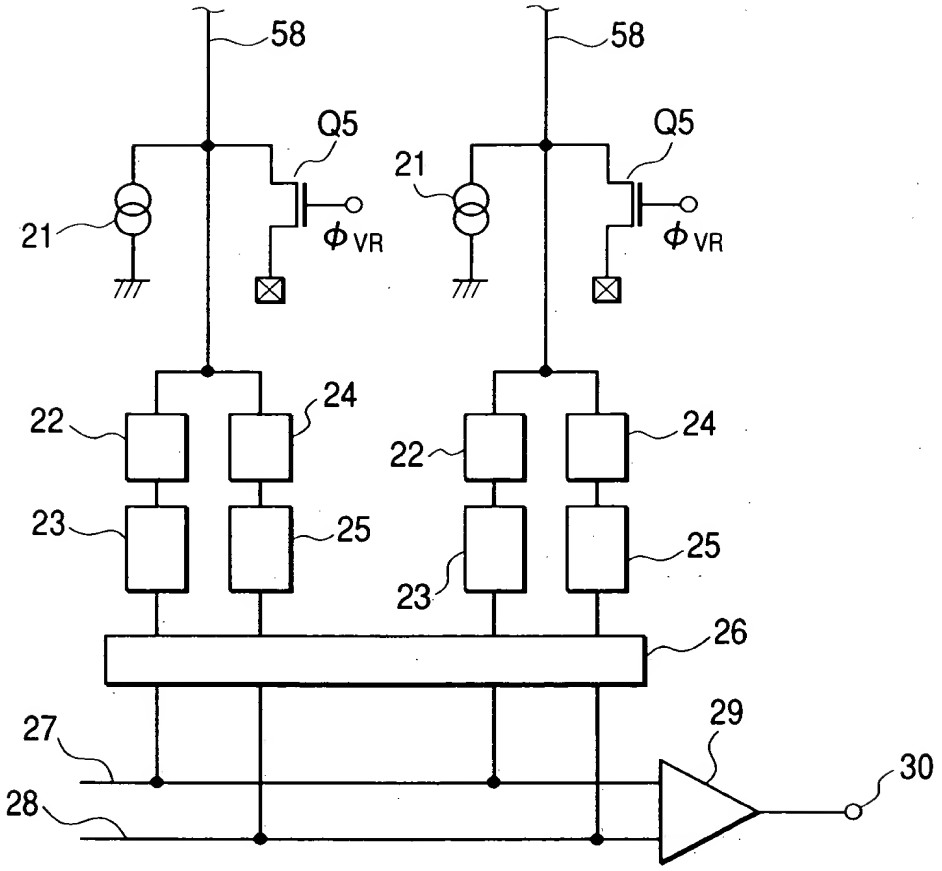

FIG. 5

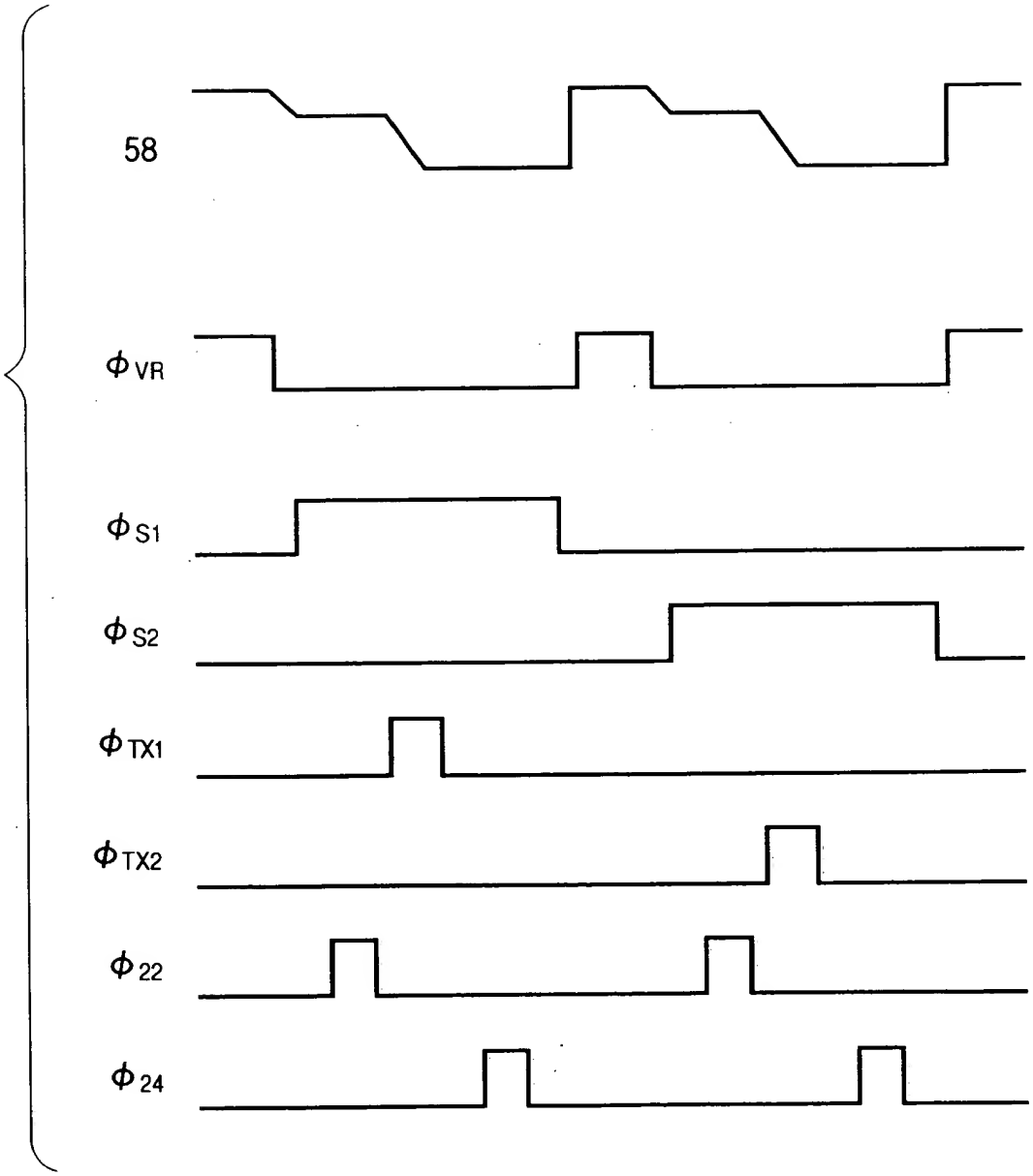

FIG. 6

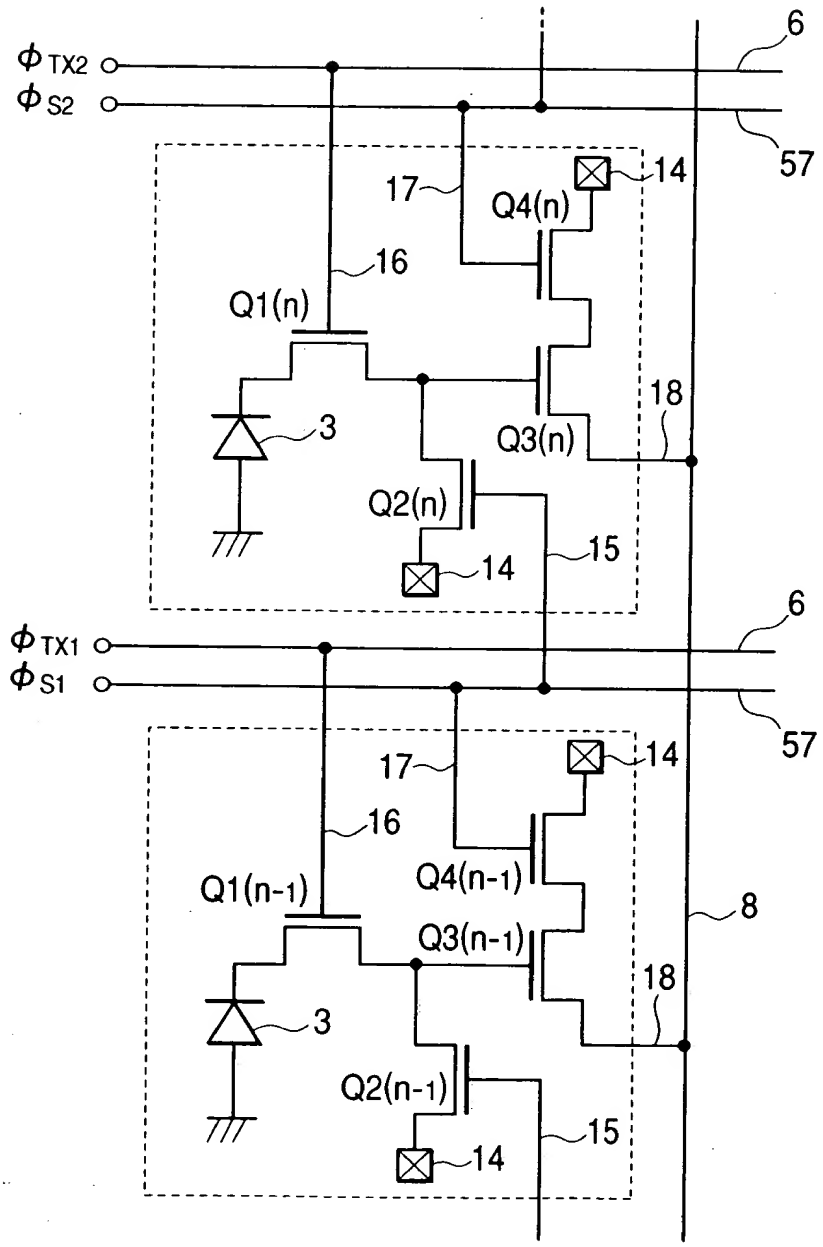
φTX2
φS2
φTX1
φS1
6
57
14
17
Q4(n)
16
Q1(n)
18
3
Q3(n)
Q2(n)
15
Q1(n-1)
Q4(n-1)
8
Q3(n-1)
Q2(n-1)

FIG. 7

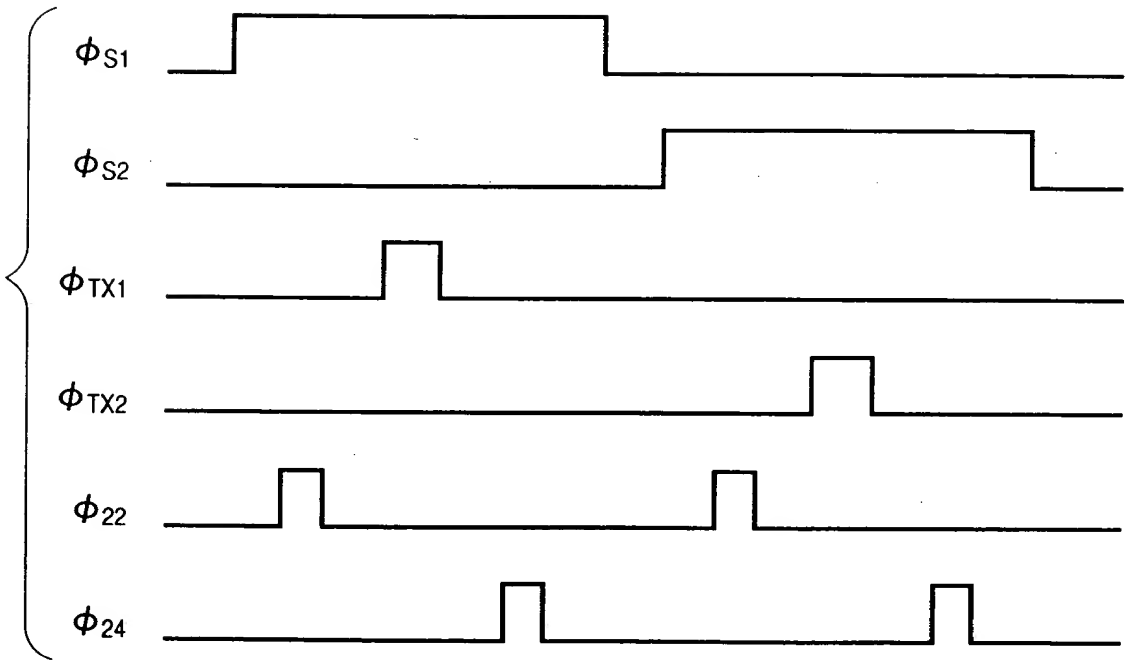

FIG. 8

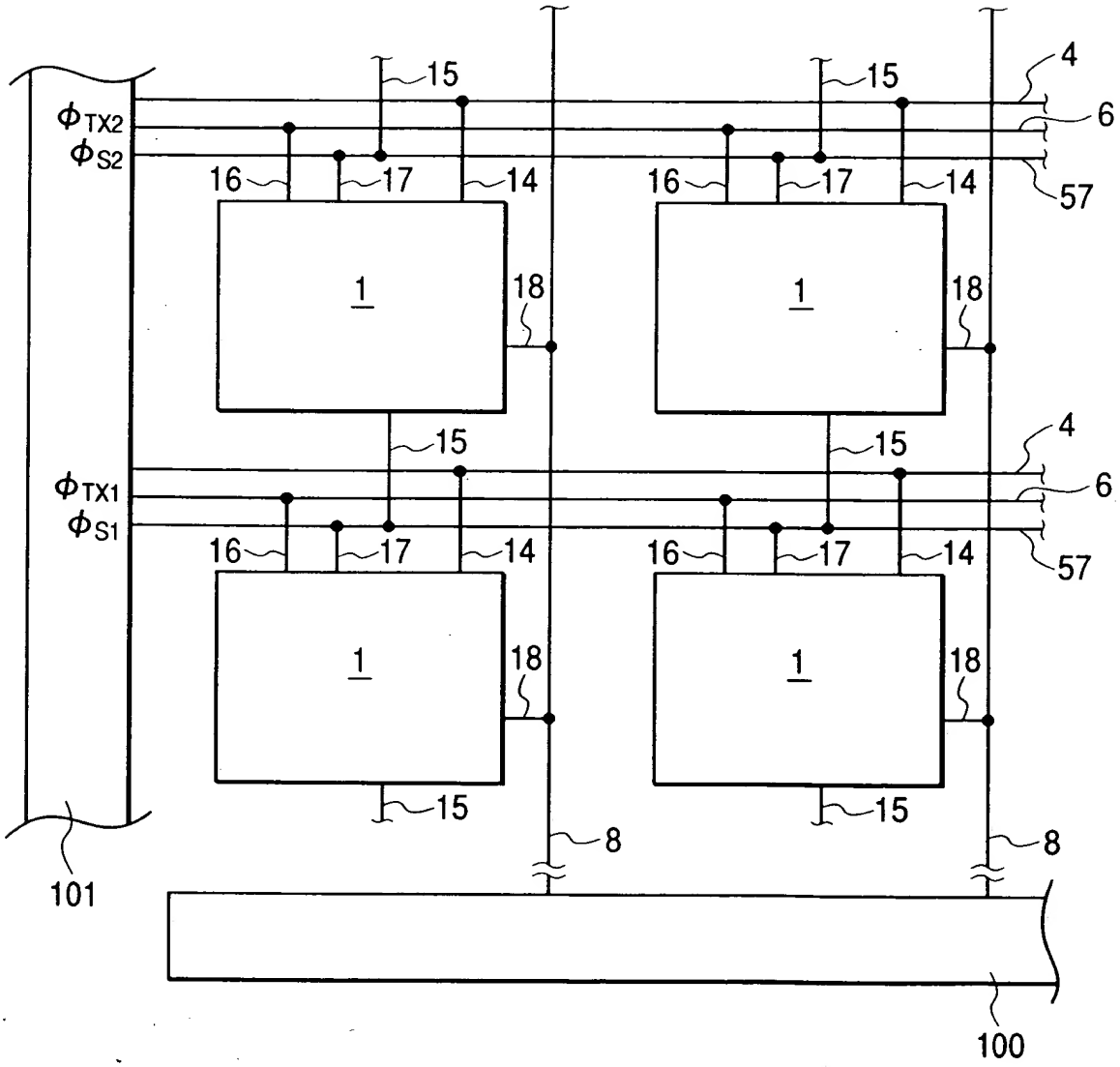

FIG. 9

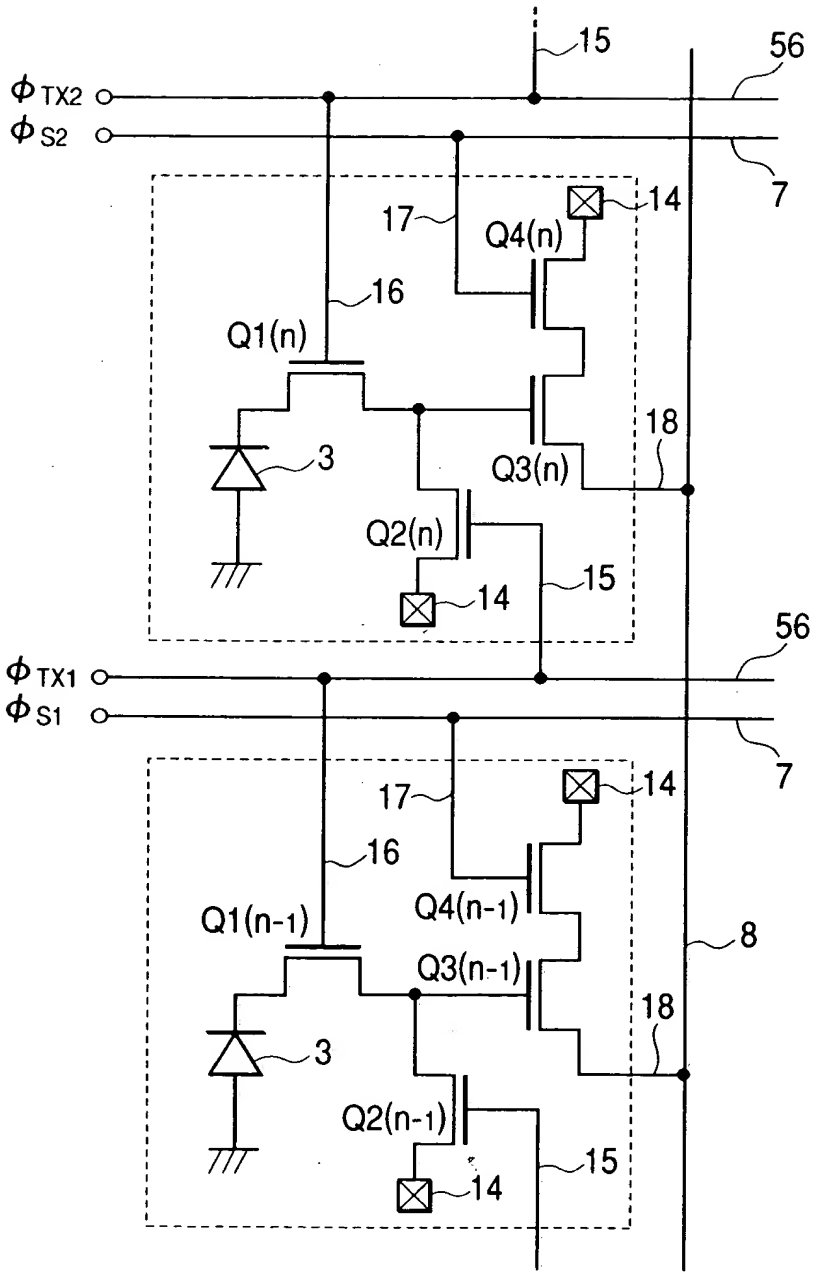
15
56
φTX2
φS2
7
17
Q4(n)
14
16
Q1(n)
18
3
Q3(n)
Q2(n)
14
15
56
φTX1
φS1
7
17
14
16
Q1(n-1)
Q4(n-1)
8
Q3(n-1)
18
3
Q2(n-1)
15
14

FIG. 10

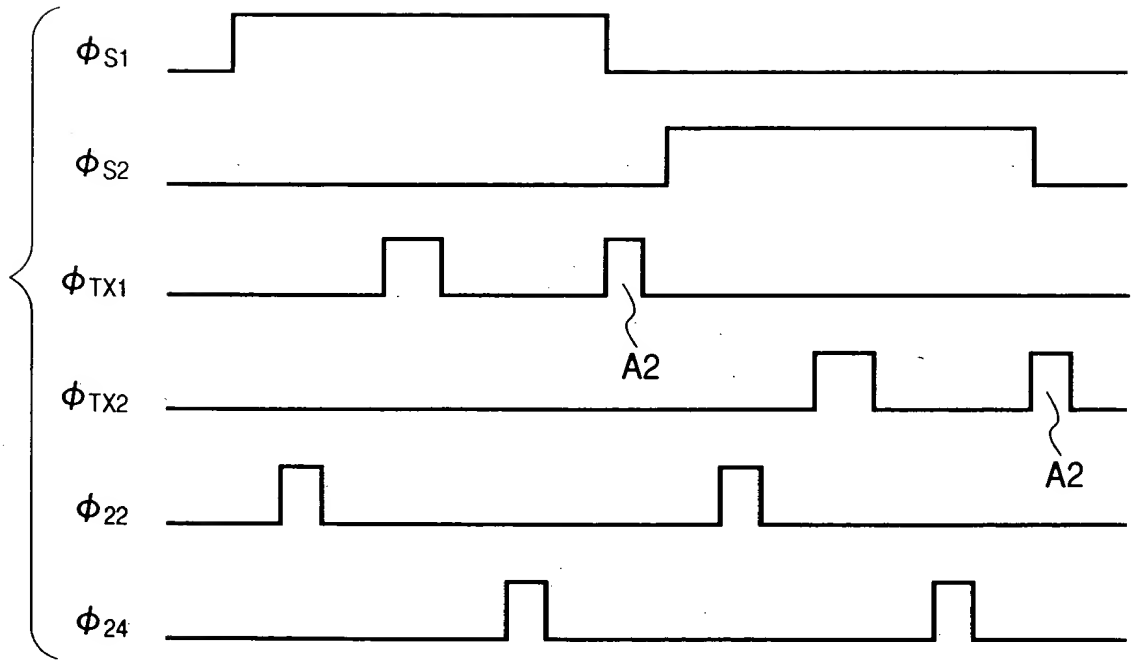

FIG. 11

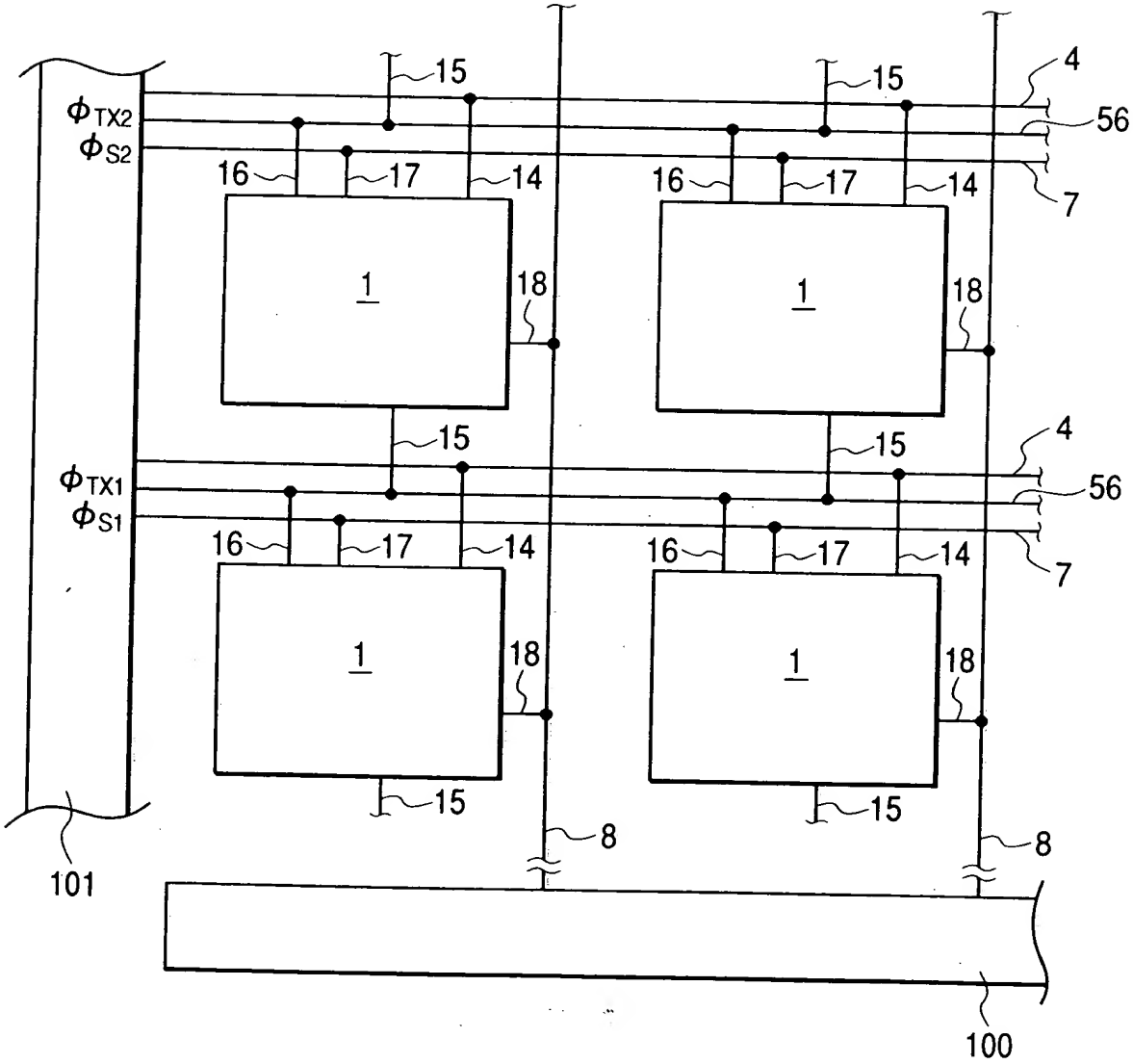

FIG. 12

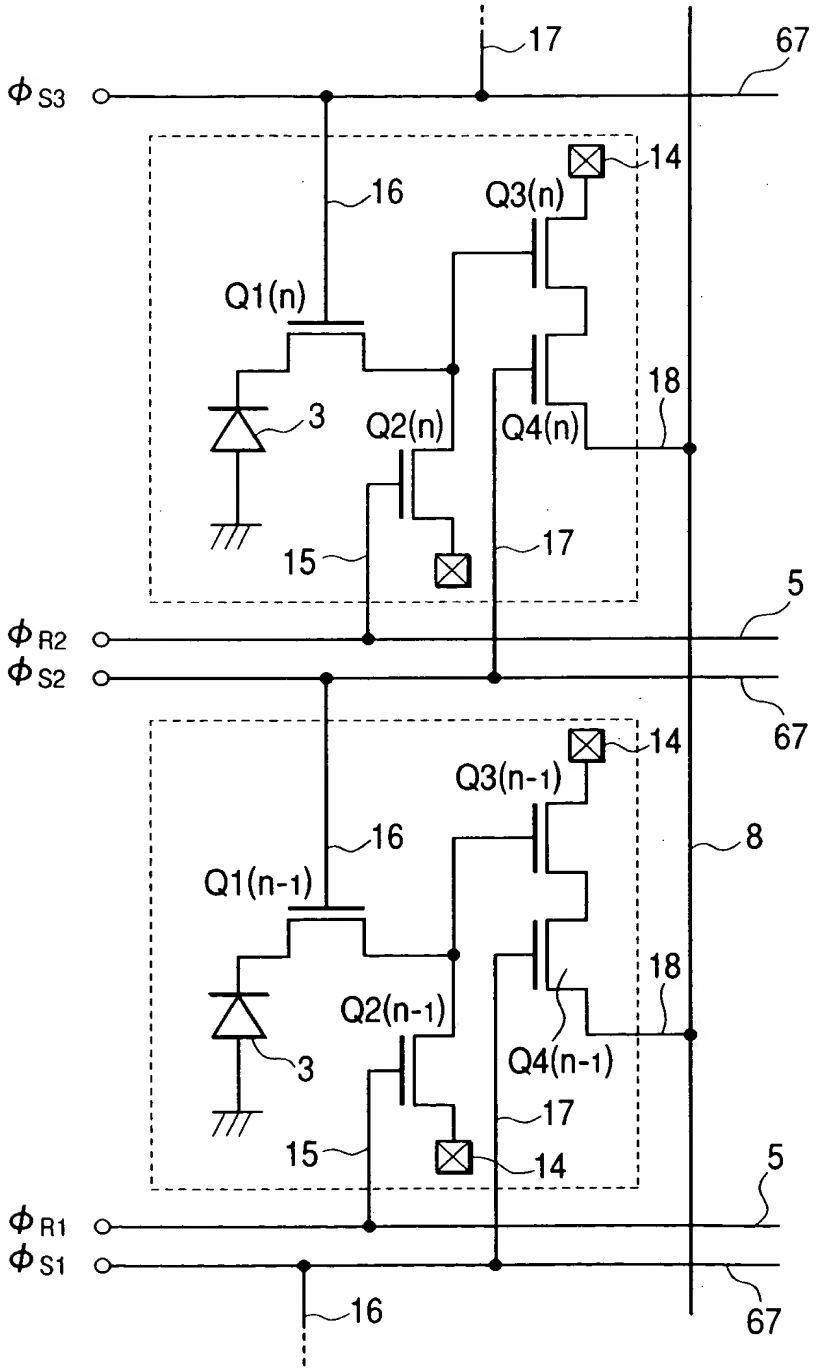
17
67
ϕ_{S3}
14
16
Q3(n)
Q1(n)
18
3
Q2(n)
Q4(n)
15
17
5
ϕ_{R2}
ϕ_{S2}
67
14
Q3(n-1)
16
8
Q1(n-1)
18
Q2(n-1)
3
Q4(n-1)
17
15
14
5
ϕ_{R1}
ϕ_{S1}
16
67

FIG. 13

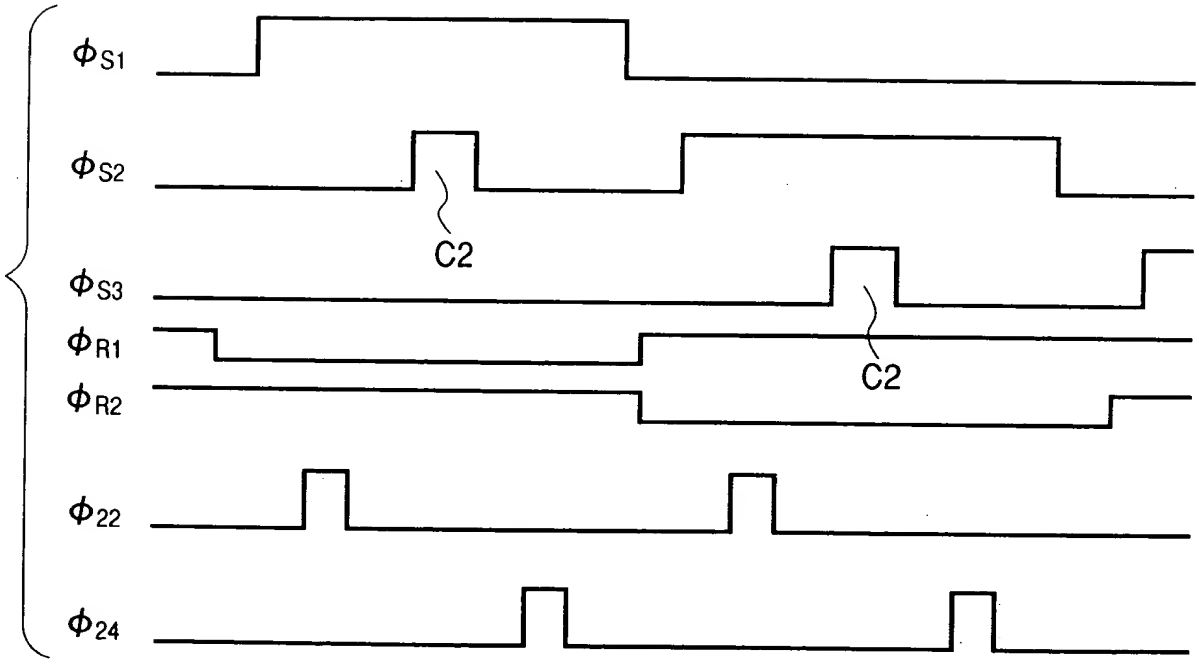

FIG. 14

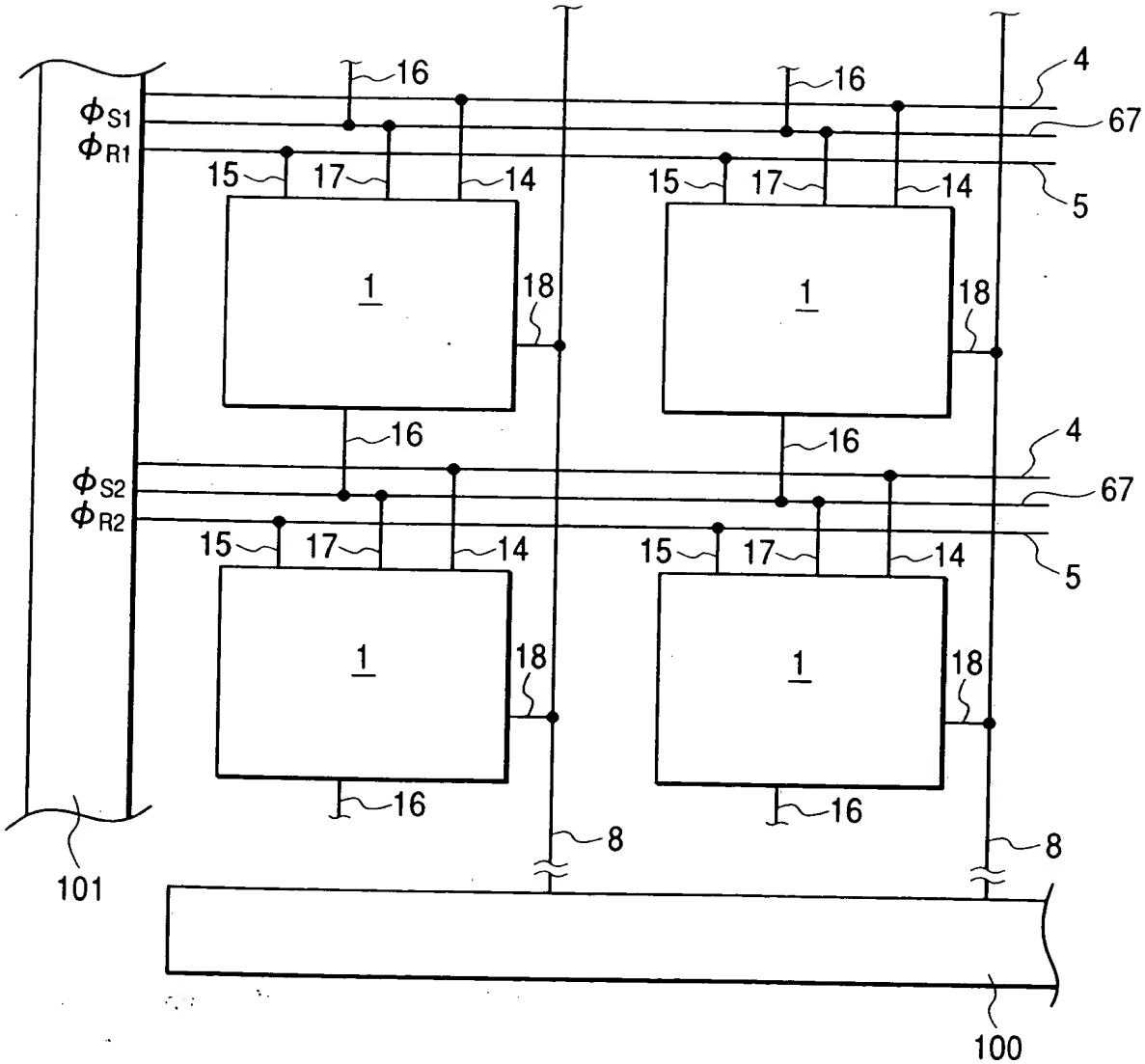

FIG. 15

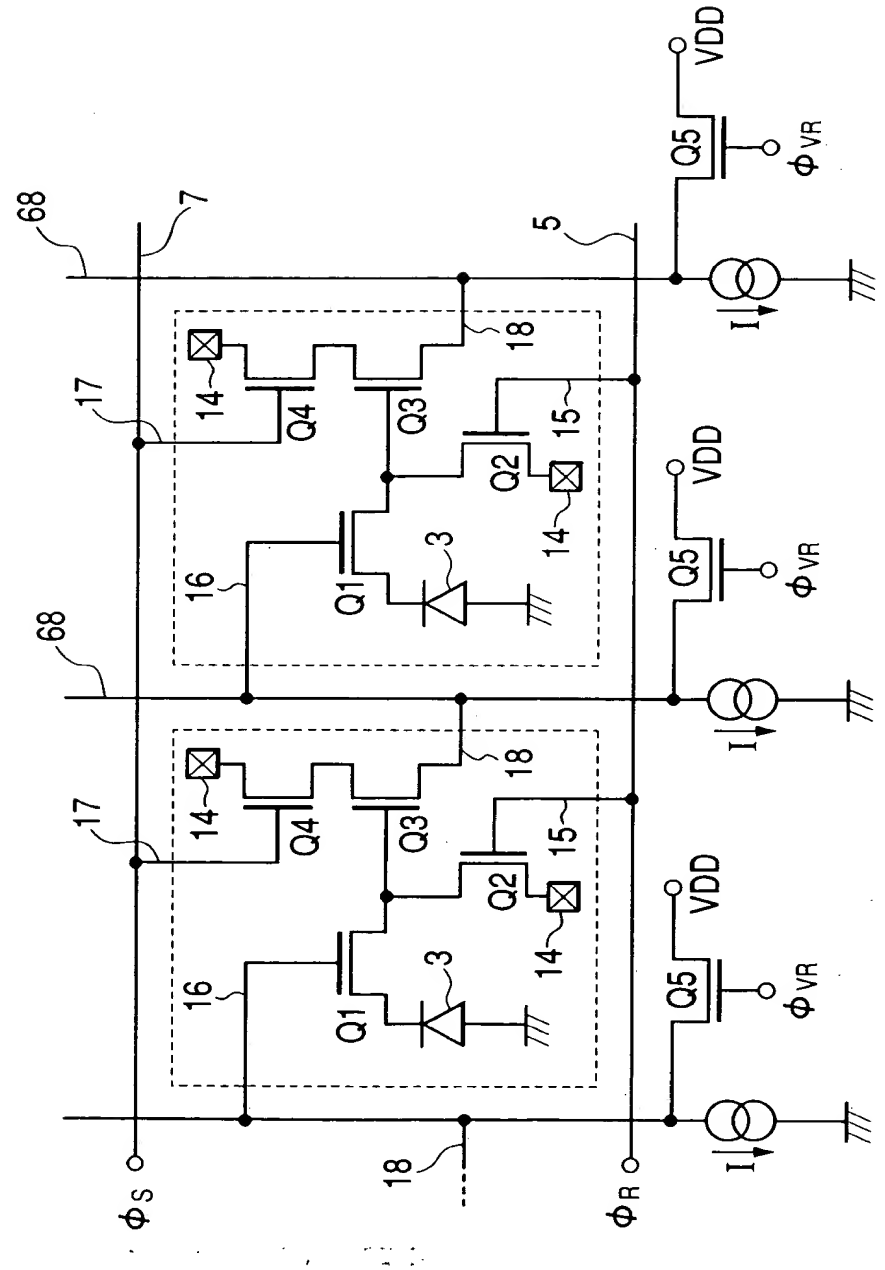

FIG. 16

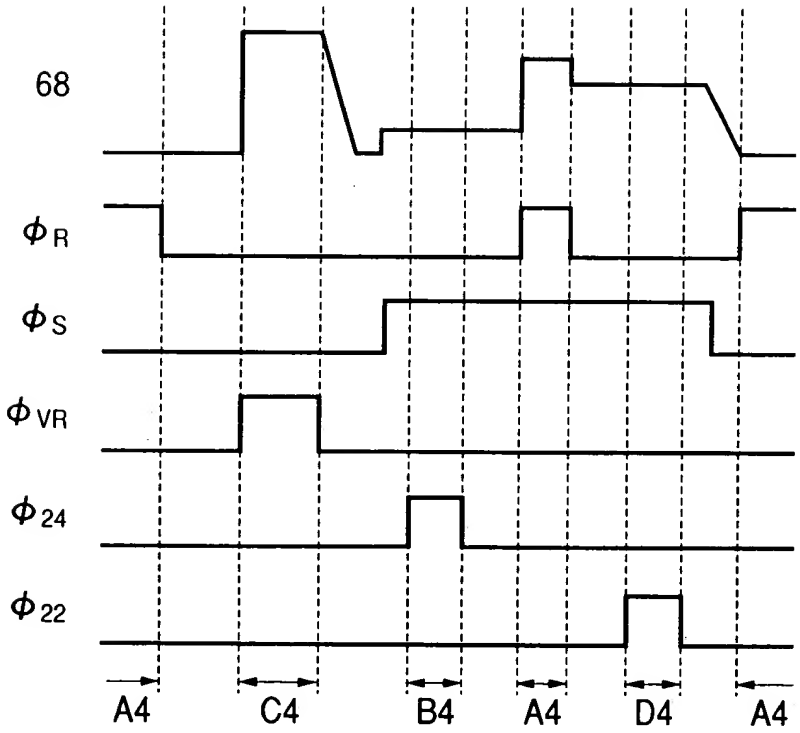

FIG. 17

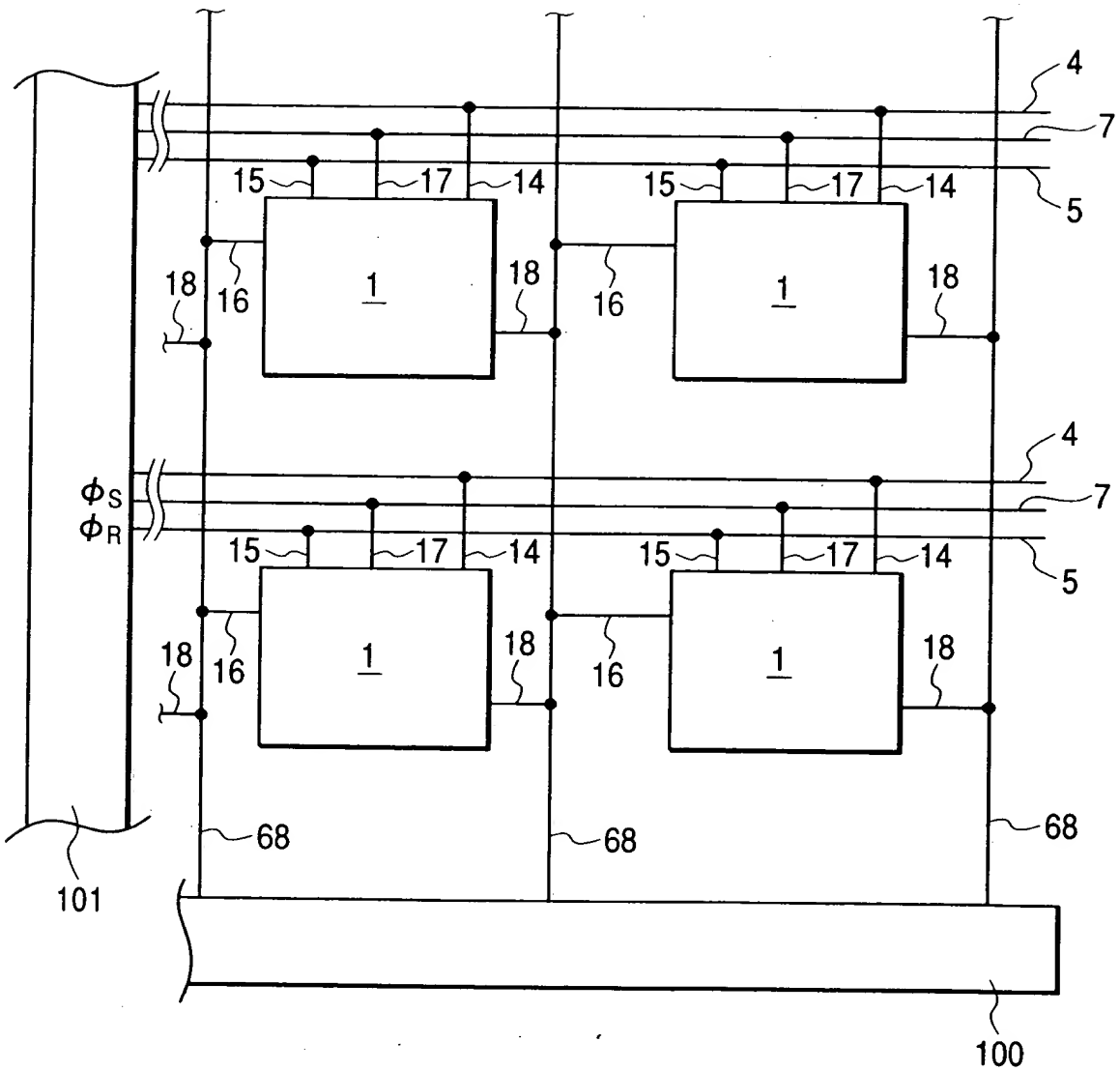

FIG. 18

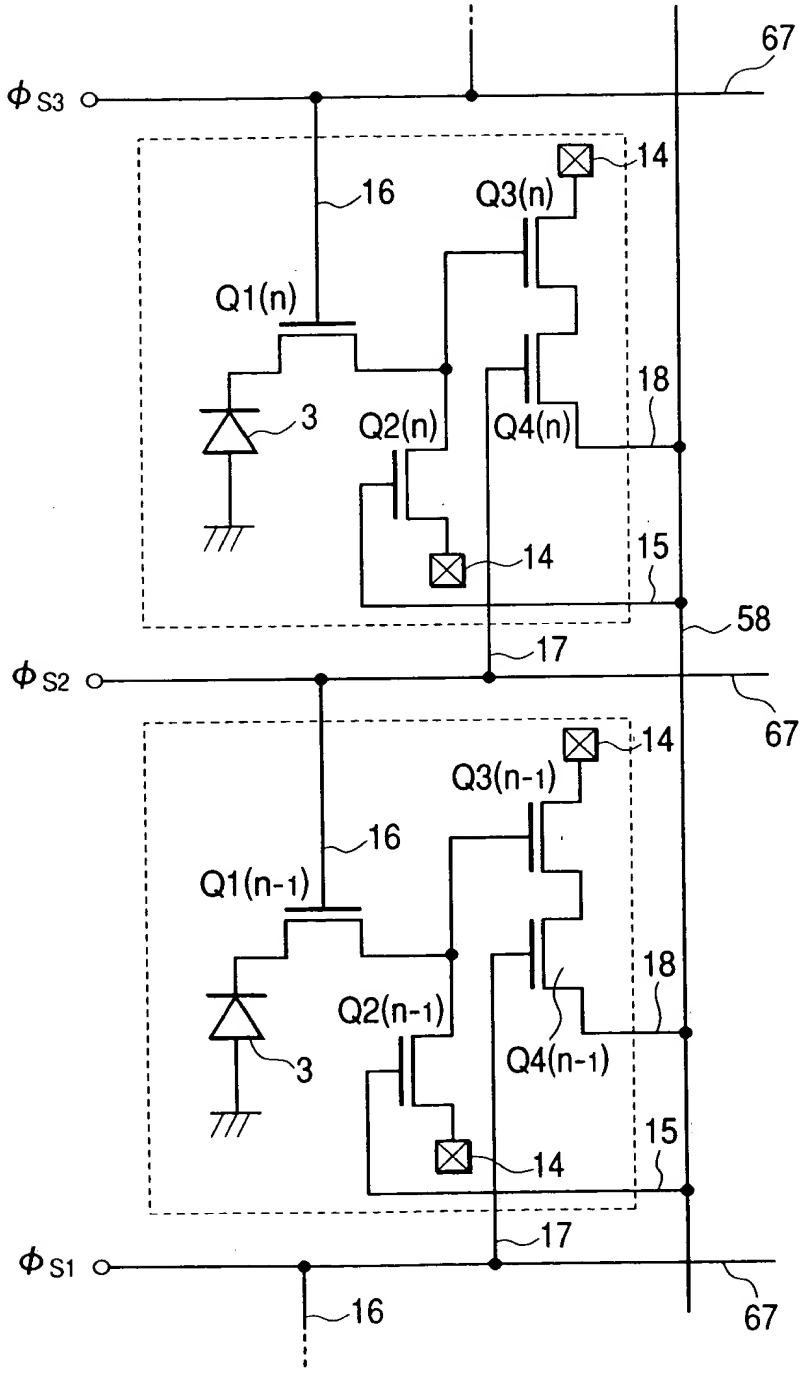
67
φS3
14
16
Q3(n)
Q1(n)
18
3
Q2(n)
Q4(n)
14
15
58
17
φS2
67
14
Q3(n-1)
16
Q1(n-1)
18
Q2(n-1)
3
Q4(n-1)
14
15
17
φS1
16
67

FIG. 19

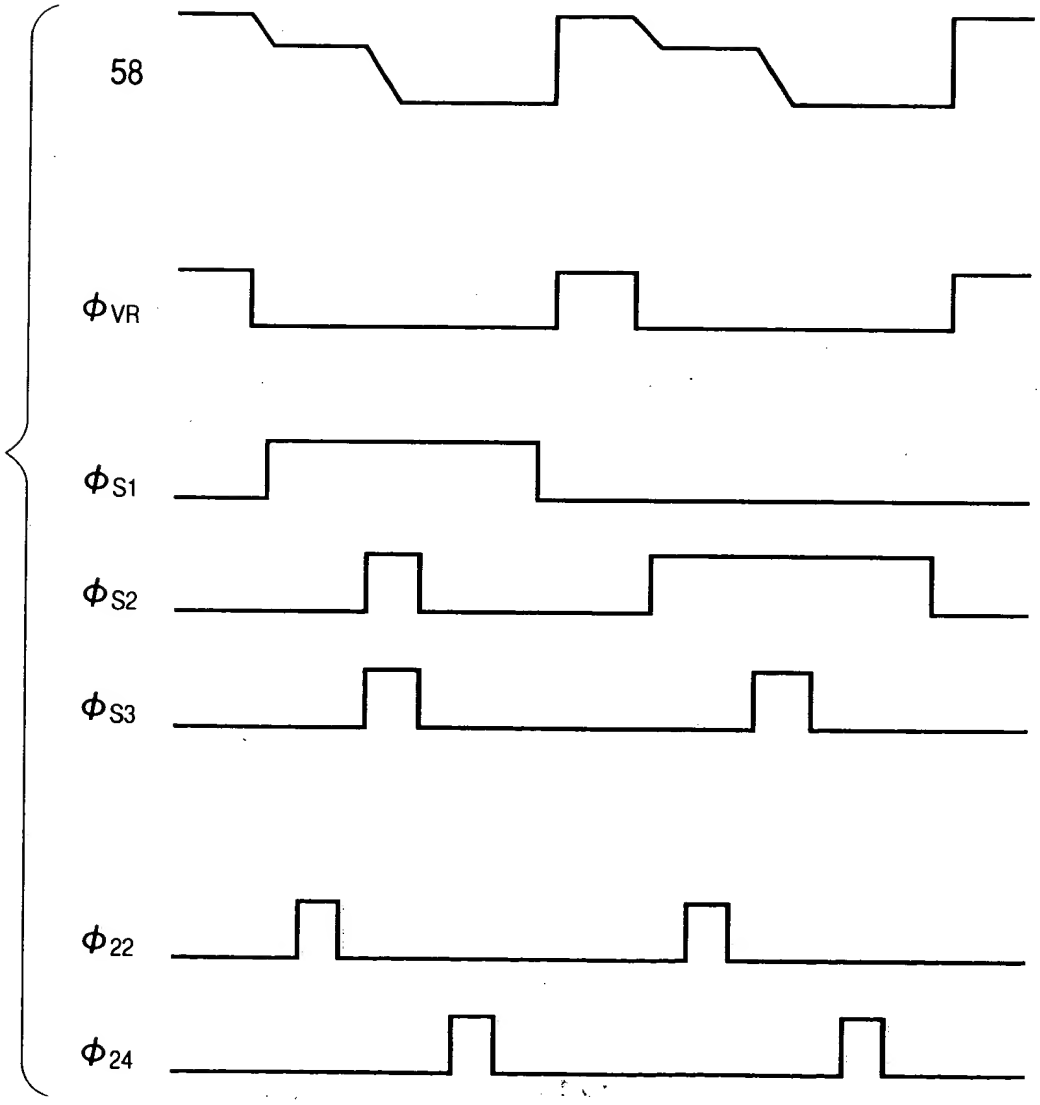

FIG. 20

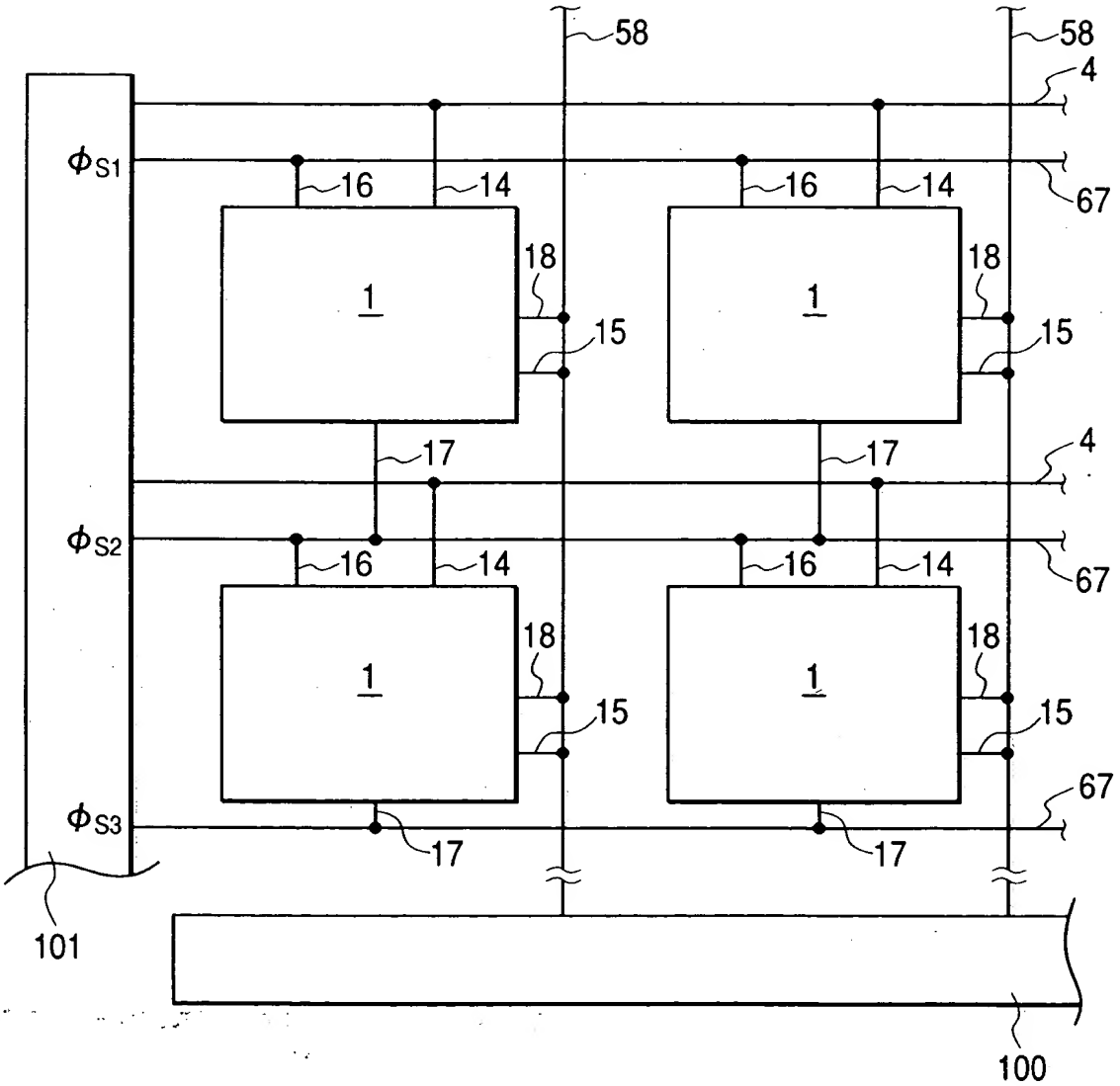
58
58
4
ϕ_{S1}
16
14
16
14
67
18
18
1
1
15
15
17
17
4
ϕ_{S2}
16
14
16
14
67
18
18
1
1
15
15
67
ϕ_{S3}
17
17
101
100

FIG. 21

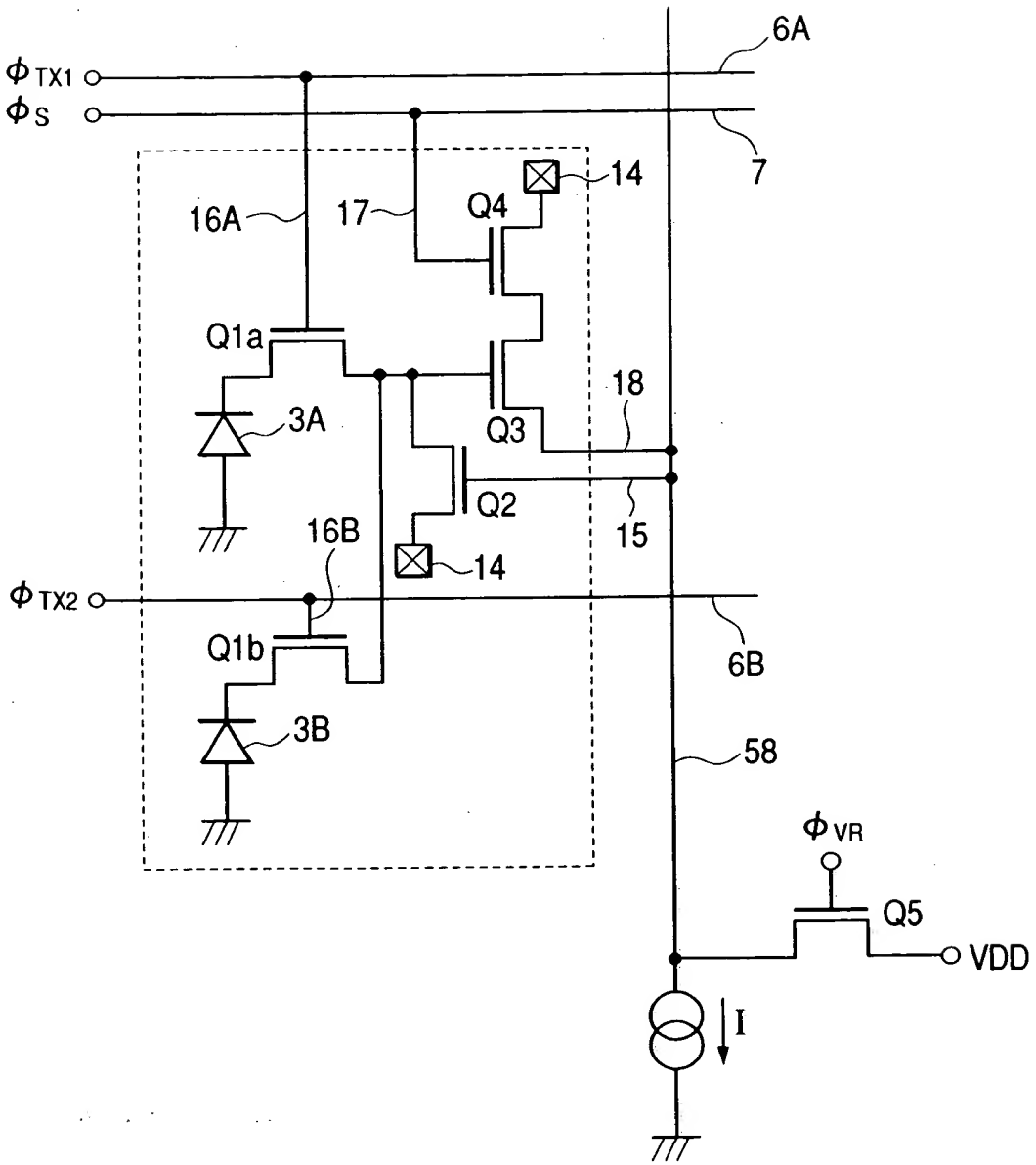
6A
φTX1
φS
7
14
16A
17
Q4
Q1a
18
3A
Q3
Q2
15
16B
14
φTX2
Q1b
6B
3B
58
φVR
Q5
VDD
I

FIG. 22

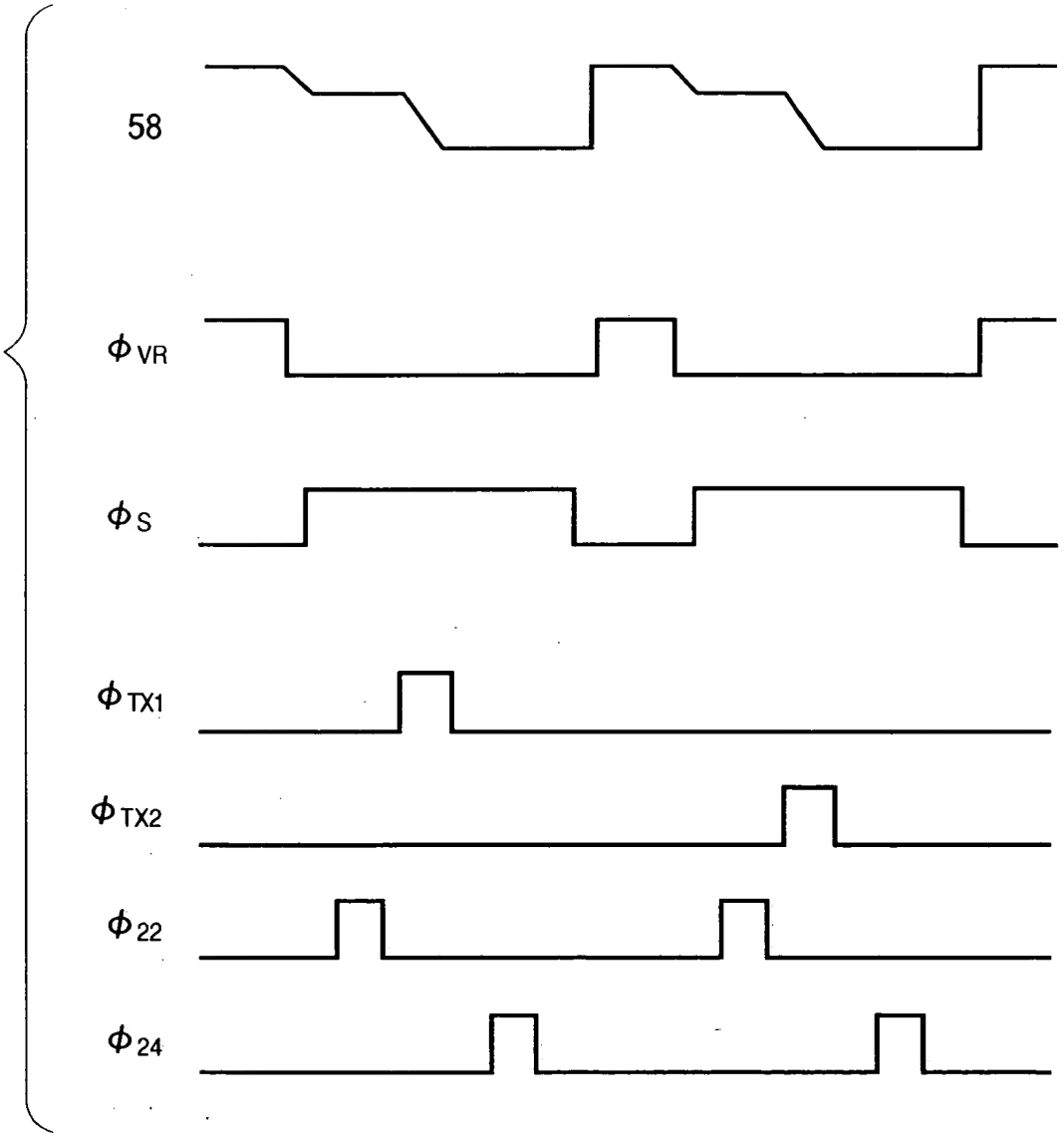

FIG. 23

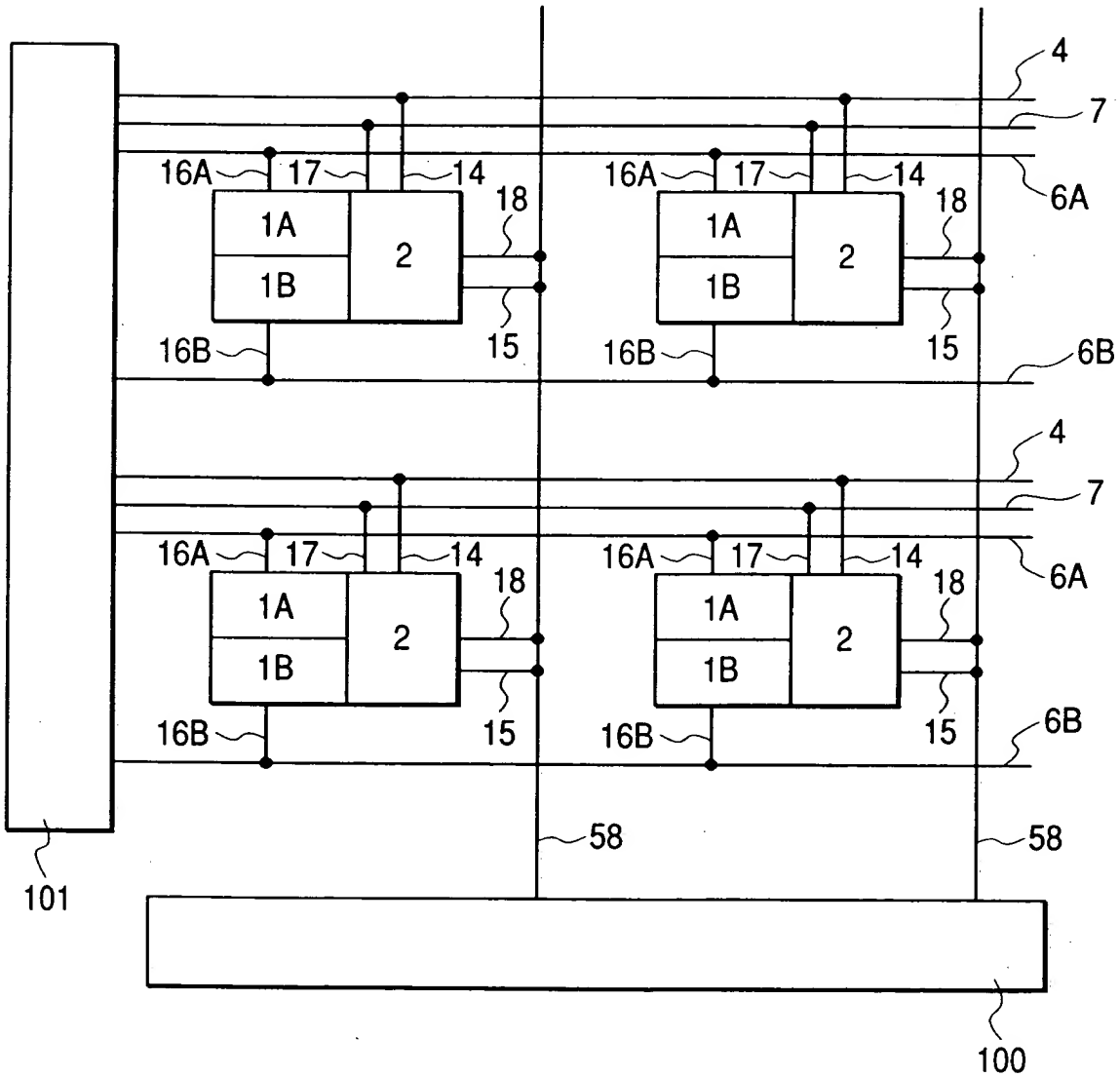

FIG. 24

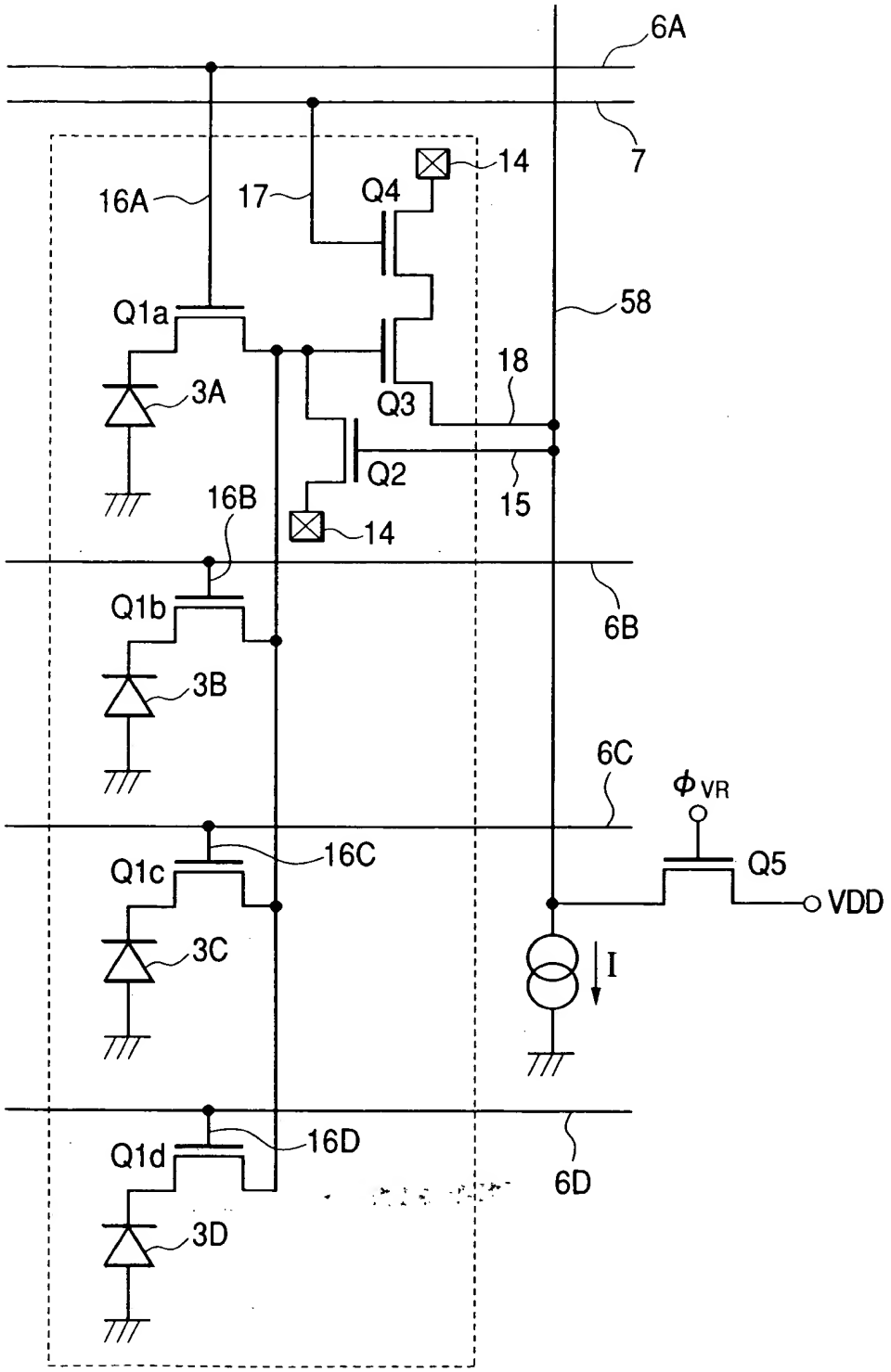
6A
7
14
16A
17
Q4
58
Q1a
18
3A
Q3
Q2
15
16B
14
6B
Q1b
3B
6C
ϕ_{VR}
Q5
VDD
16C
Q1c
3C
I
16D
Q1d
6D
3D

FIG. 25

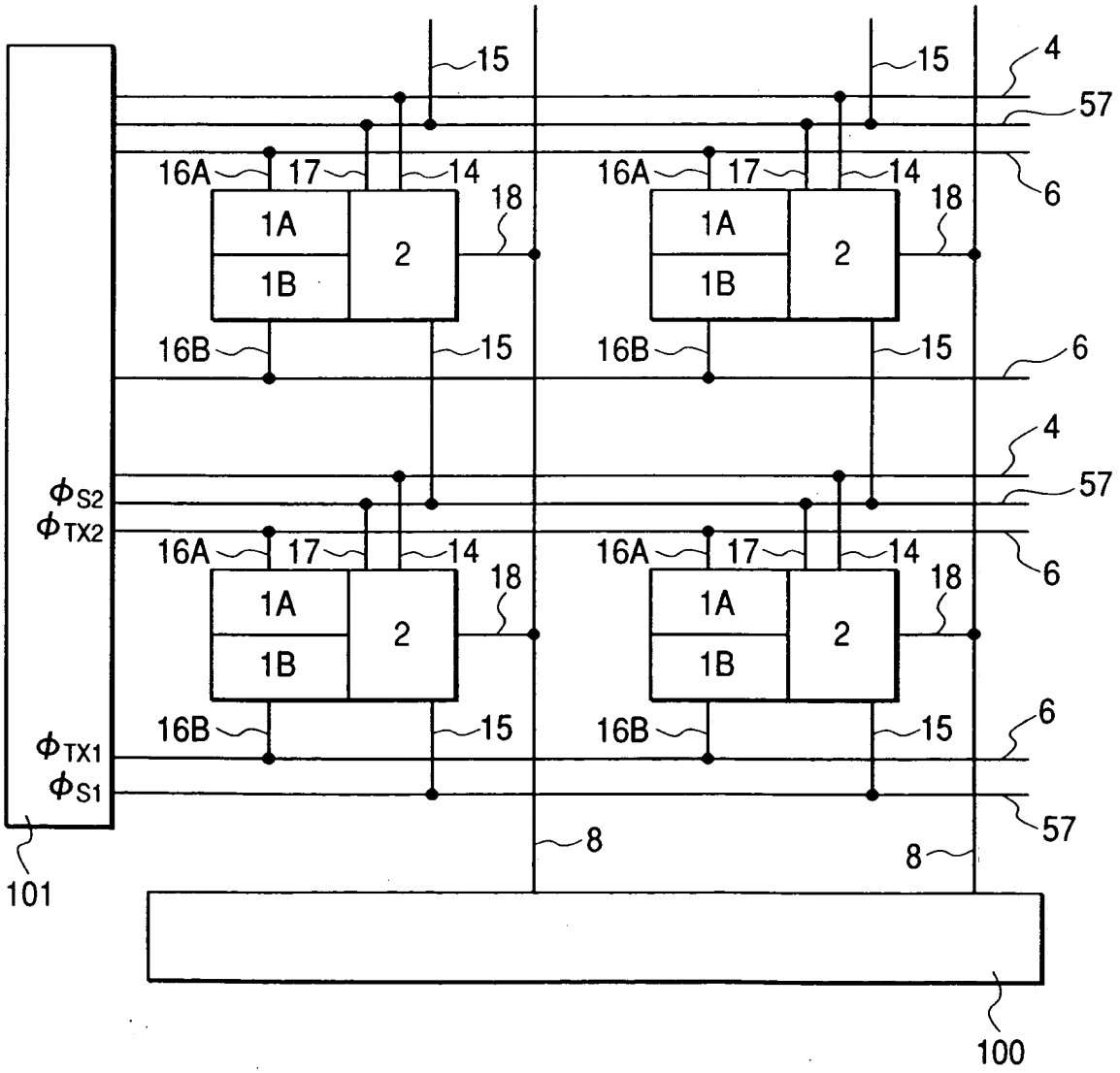
15
15
4
57
6
16A
17
14
18
1A
1B
2
16B
ϕ_{S2}
ϕ_{TX2}
ϕ_{TX1}
ϕ_{S1}
8
101
100

FIG. 26

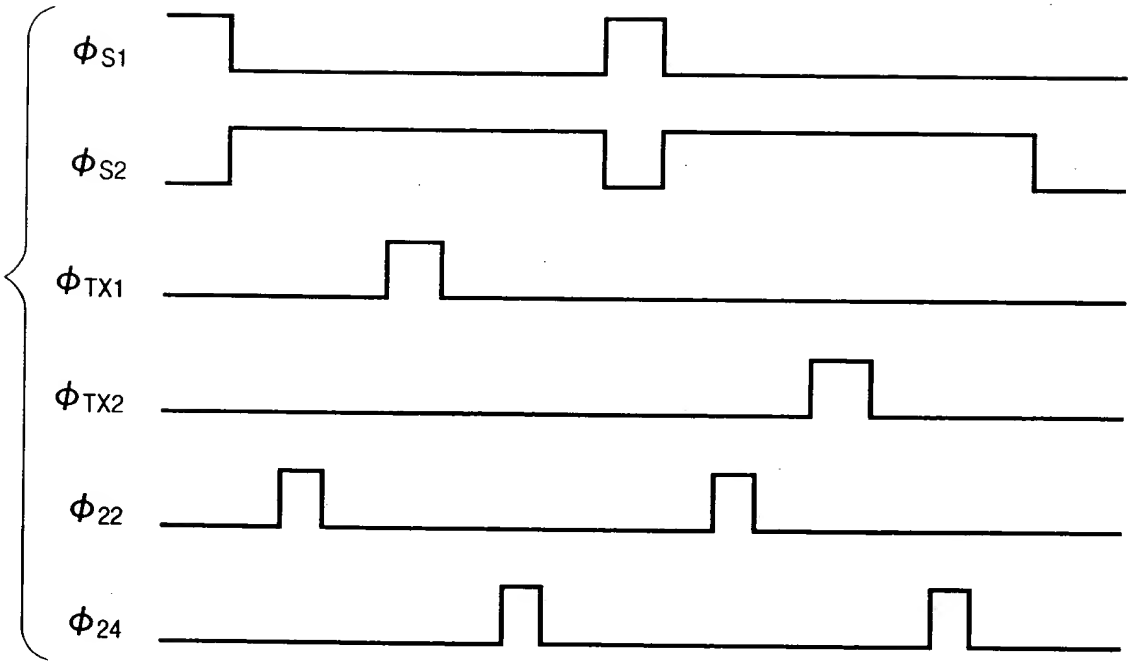

FIG. 27

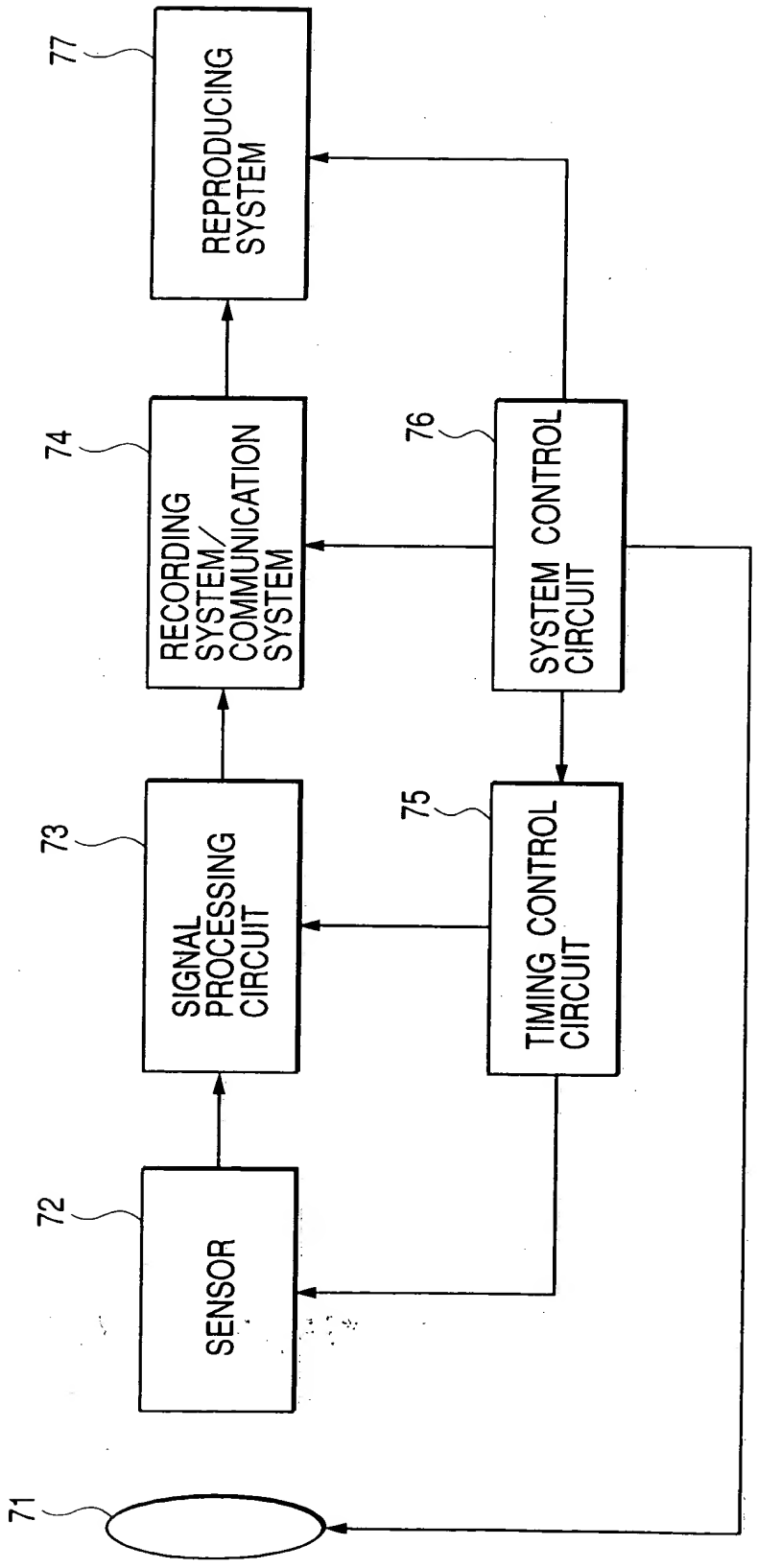
71
72
SENSOR
73
SIGNAL PROCESSING CIRCUIT
74
RECORDING SYSTEM/ COMMUNICATION SYSTEM
75
TIMING CONTROL CIRCUIT
76
SYSTEM CONTROL CIRCUIT
77
REPRODUCING SYSTEM

FIG. 28 PRIOR ART

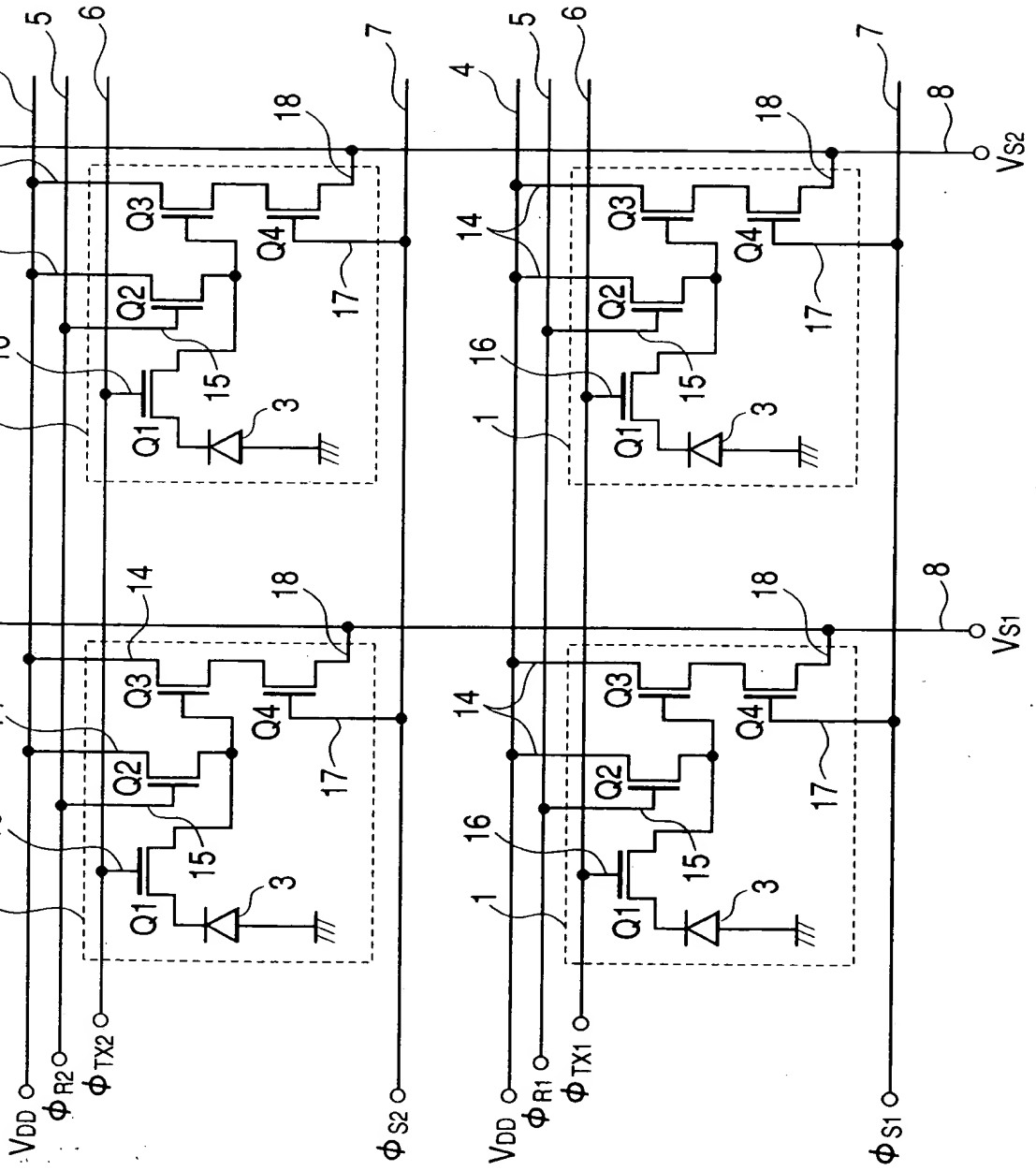

FIG. 29

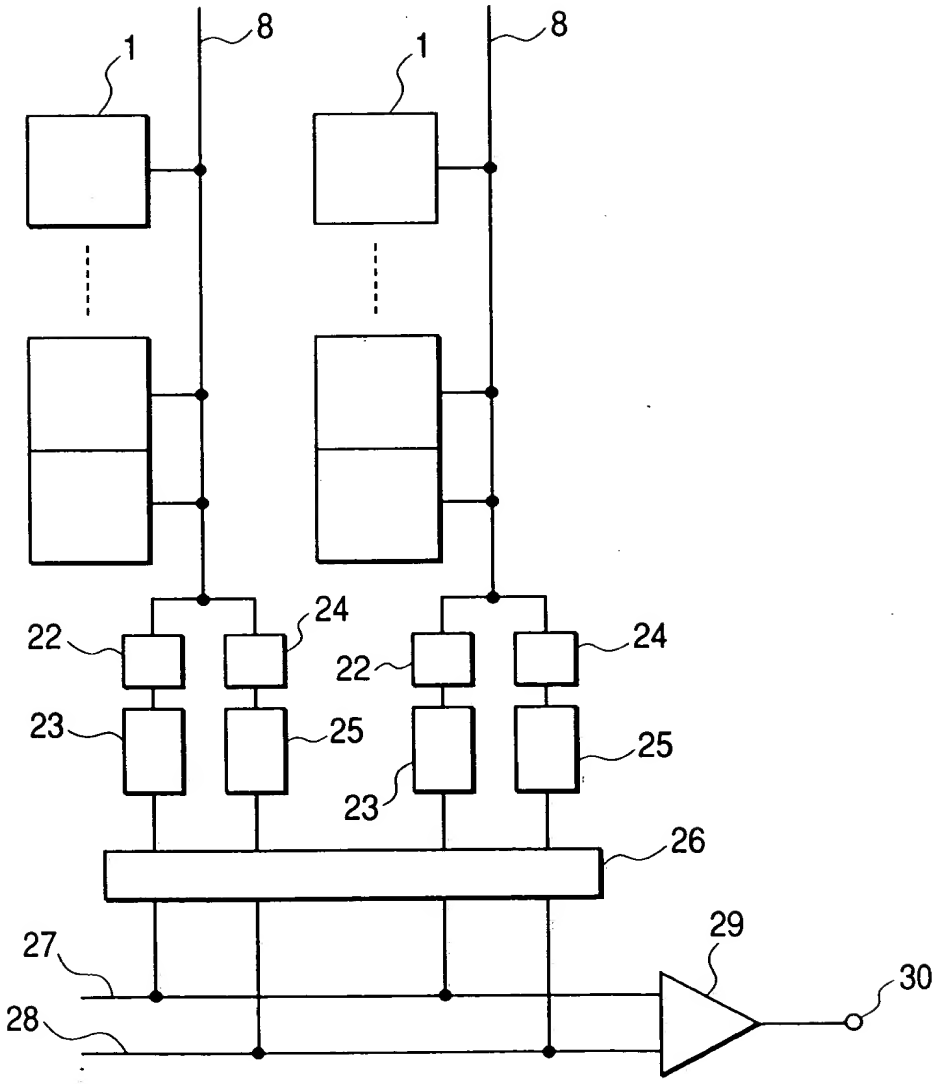

FIG. 30

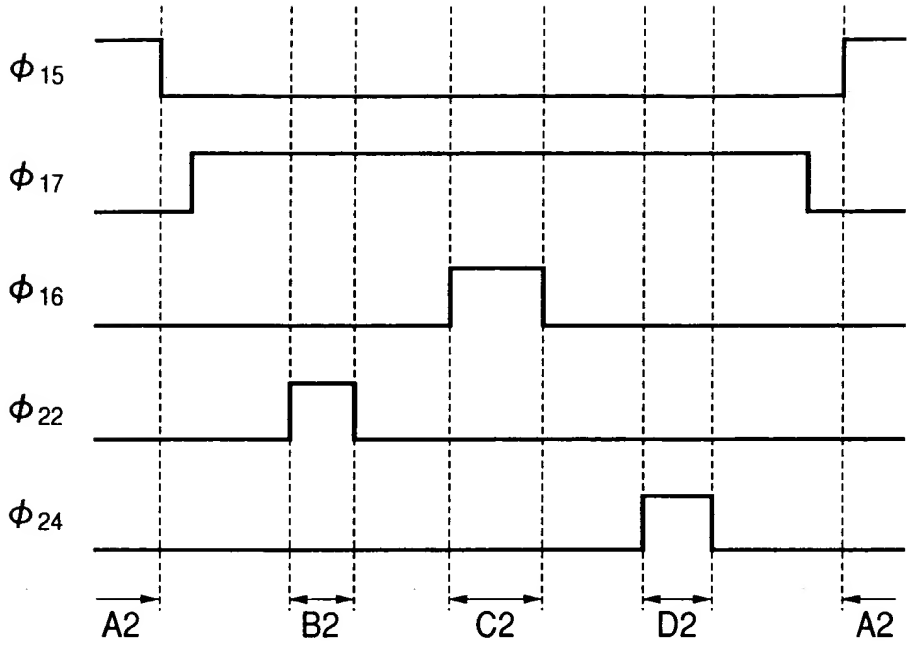
Φ15
Φ17
Φ16
Φ22
Φ24
A2
B2
C2
D2
A2

FIG. 31

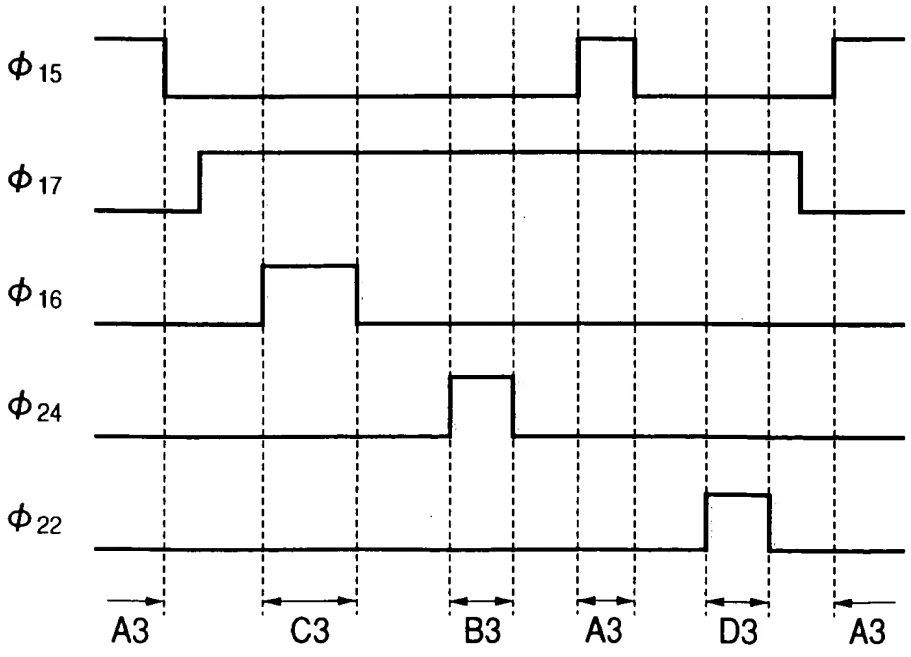
Φ15
Φ17
Φ16
Φ24
Φ22
A3
C3
B3
A3
D3
A3

FIG. 32

	PERIOD A	PERIOD B	PERIOD C	PERIOD D
n TH ROW SELECTING SWITCH LINE	—	ON	—	ON
n TH ROW RESET SWITCH LINE	ON	OFF *	OFF *	OFF *
n TH ROW TRANSFER SWITCH LINE	OFF	OFF	ON	OFF
OUTPUT LINE	—	float	—	float
n−1 TH ROW SELECTING SWITCH LINE	—	OFF	—	OFF
n−1 TH ROW RESET SWITCH LINE	—	—	—	—
n−1 TH ROW TRANSFER SWITCH LINE	—	—	—	—
n+1 TH ROW SELECTING SWITCH LINE	—	OFF	—	OFF
n+1 TH ROW RESET SWITCH LINE	—	—	—	—
n+1 TH ROW TRANSFER SWITCH LINE	OFF	OFF	OFF	OFF

FIG. 33